Prior Art: Memory Bus 0

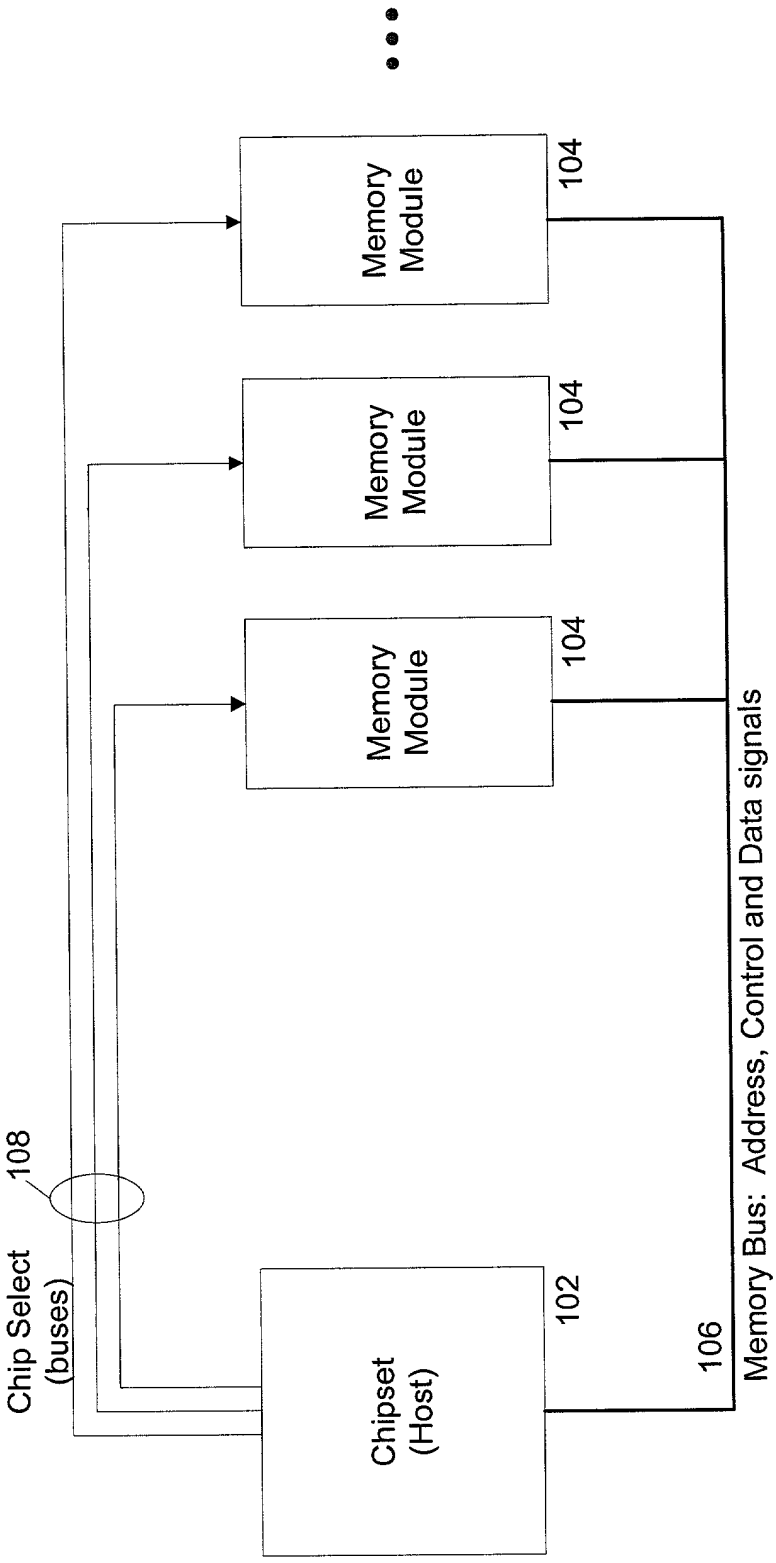

Figure 1

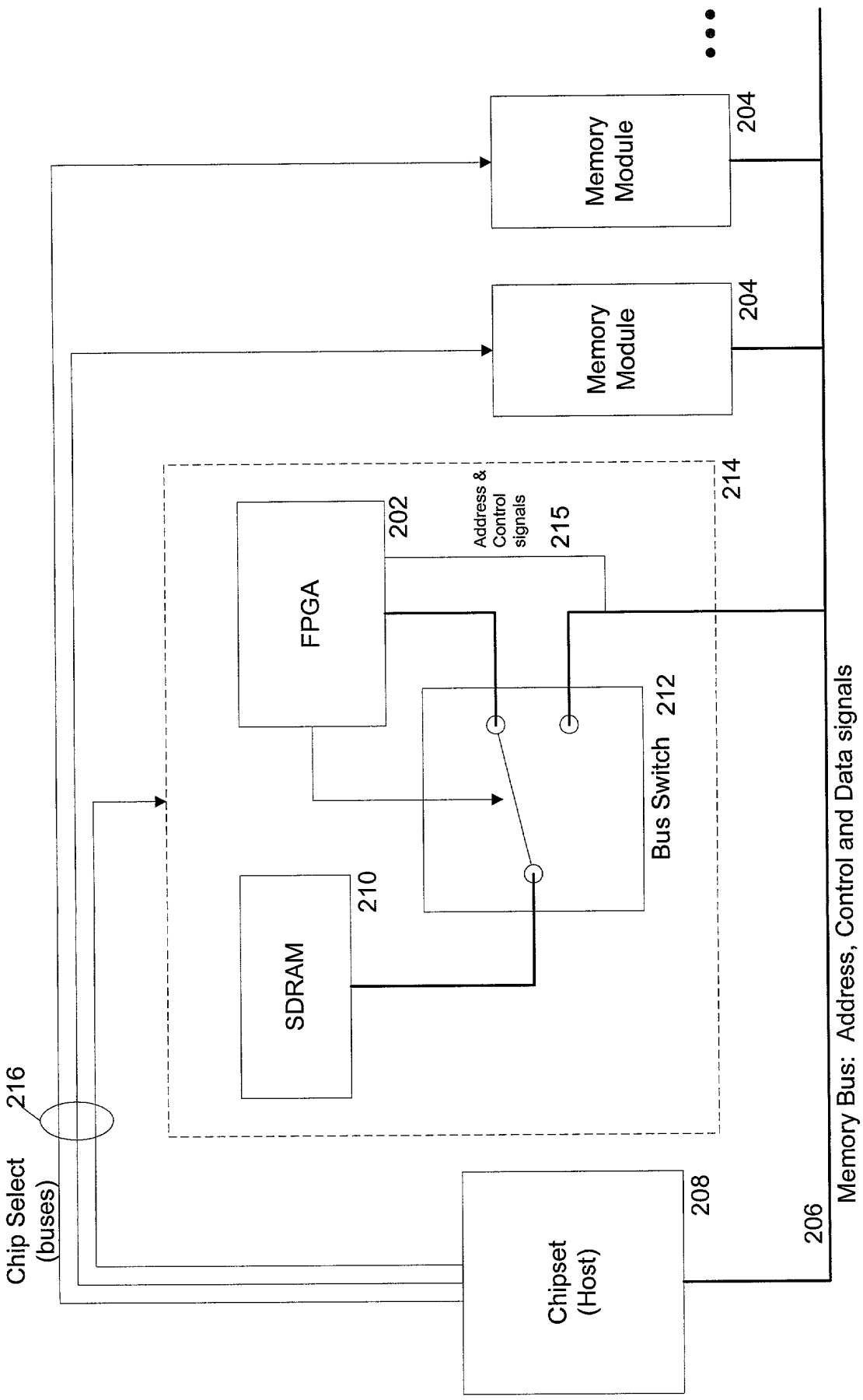
Memory Bus Peripheral (FPGA) Operation
Memory Module
204
Memory Module
204
214
Address & Control signals
215
FPGA
202
Bus Switch
212
SDRAM
210
216
Chip Select (buses)
Chipset (Host)
208
206
Memory Bus: Address, Control and Data signals

Figure 2

Operational Flowchart

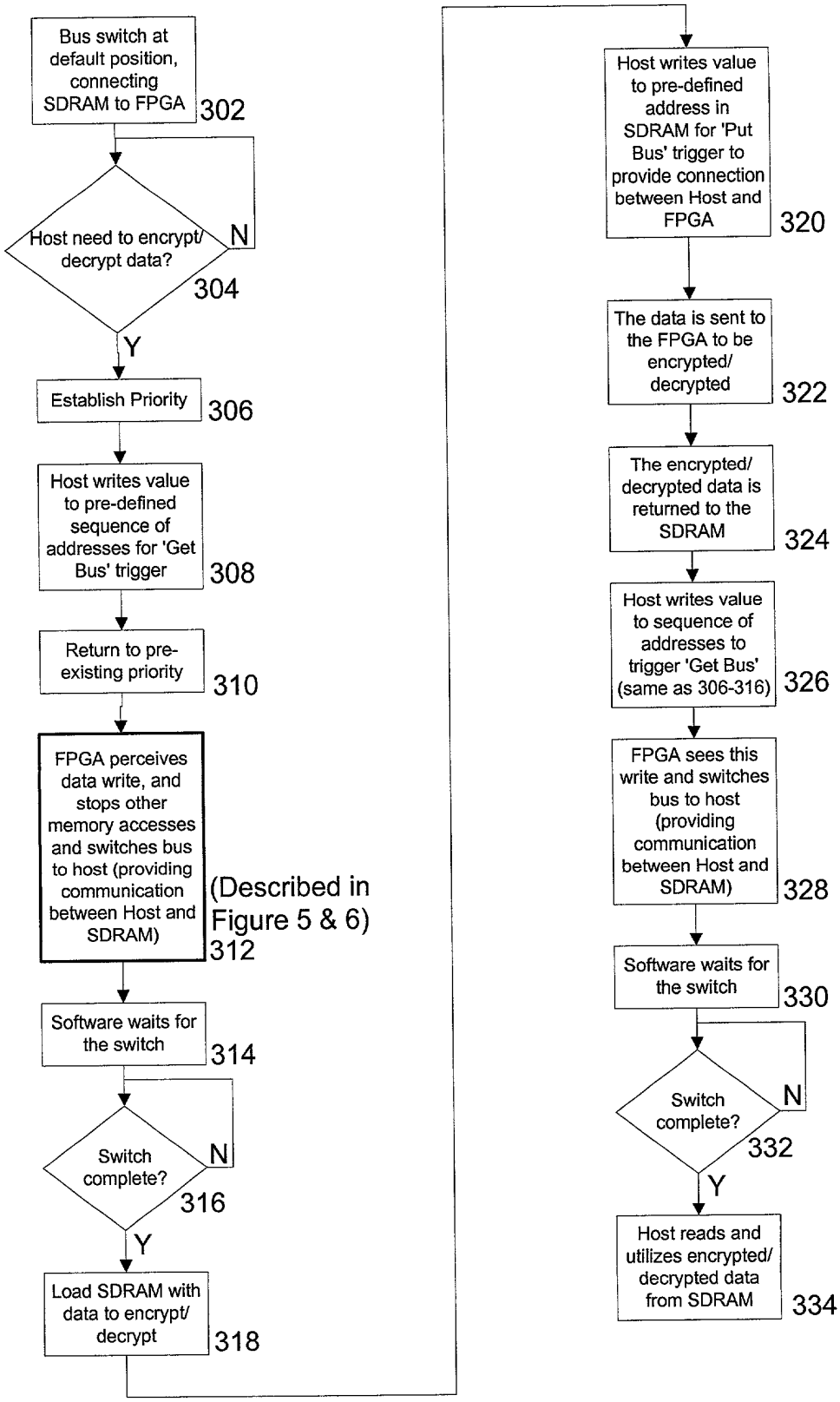

Figure 3

Example Memory Module Trigger Address Locations

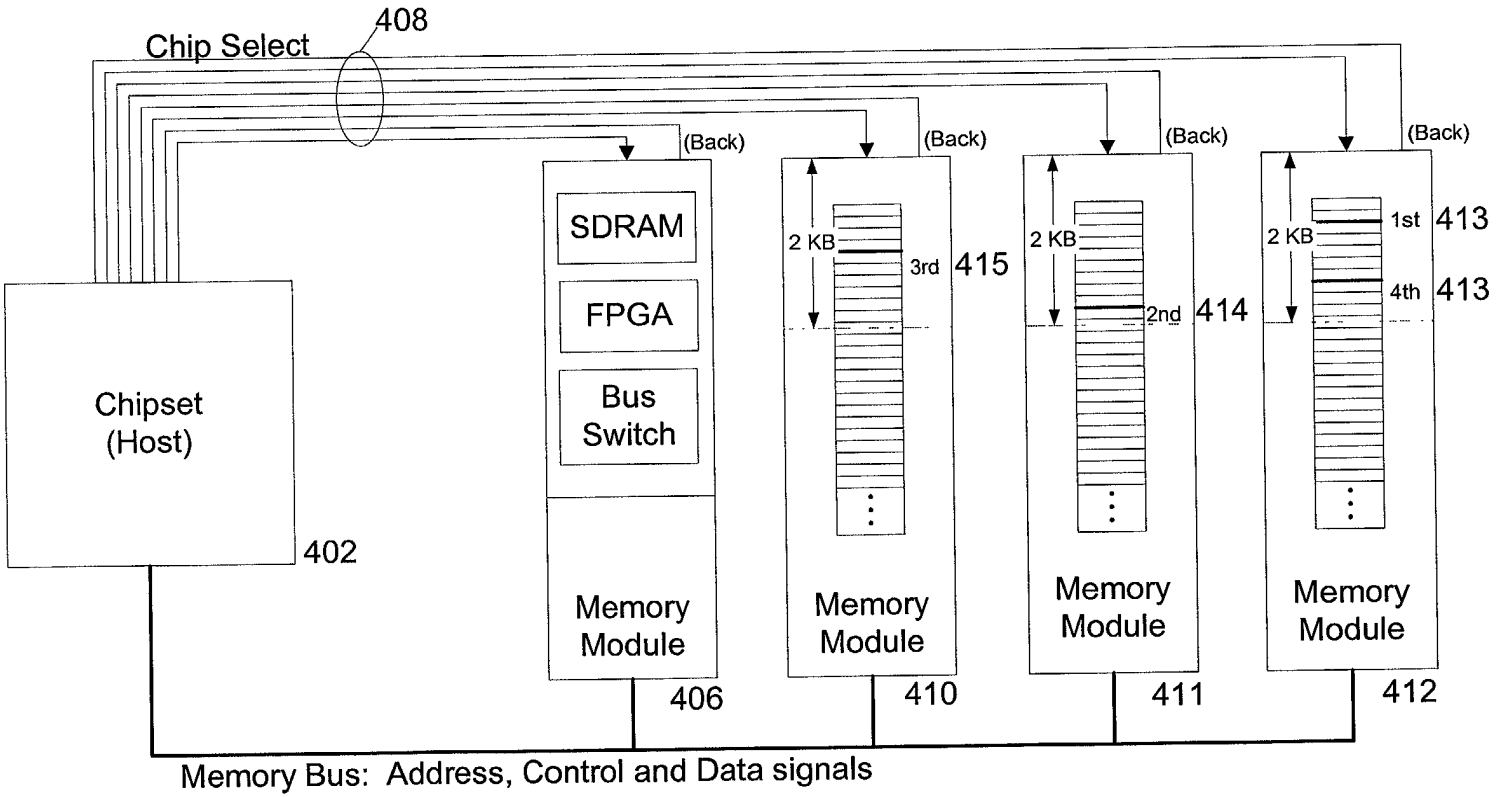

Figure 4

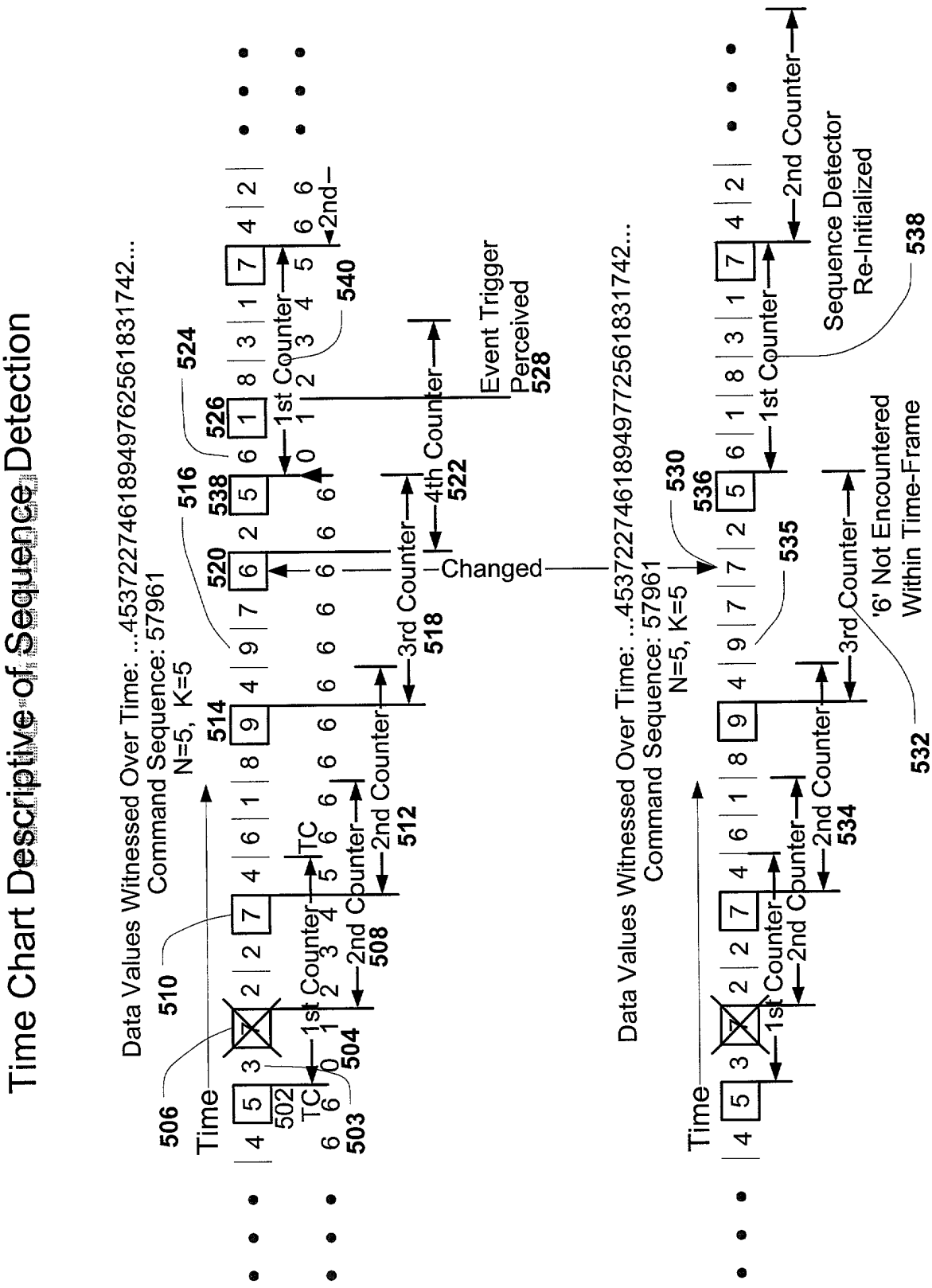
Time Chart Descriptive of Sequence Detection
Data Values Witnessed Over Time: ...4537227461894976256183174 2...
Command Sequence: 57961
N=5, K=5
Time
TC
1st Counter
2nd Counter
3rd Counter
4th Counter
Changed
Event Trigger Perceived
Sequence Detector Re-Initialized
'6' Not Encountered Within Time-Frame
502
503
504
506
508
510
512
514
516
518
520
522
524
526
528
530
532
534
535
536
538
540

Figure 5

General Schematic of Data Value Sequence Detector 600

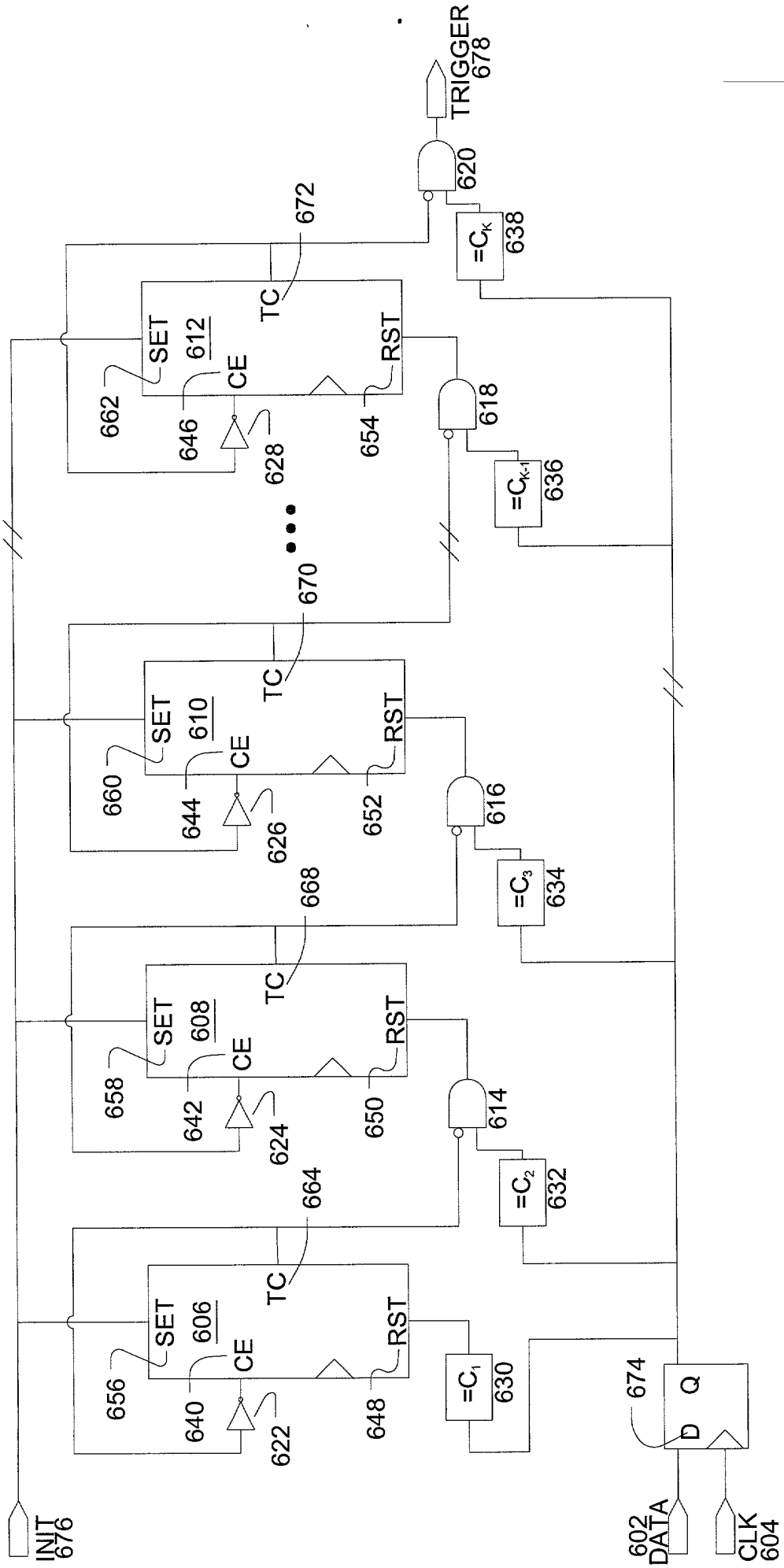

Figure 6